RESEARCH ARTICLE

An Eight-Octant bipolar junction transistor analog multiplier circuit and its applications

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Abstract: This paper presents a circuit topology for an eight-octant analog multiplier implemented using bipolar junction transistors. The proposed circuit is an extension of four-quadrant Gilbert multiplier. The possibility of multiplying three input signals using the proposed circuit is theoretically proved. A scheme to upgrade this circuit to operate for large input signals is also proposed. Theoretical results are validated through spice simulations for small input signals. The possible use of the proposed circuit as a three input mixer, three input emitter coupled logic, or two input multiplier with an enable/disable switch is shown through spice simulations.

Keywords: Eight-octant multiplier; three-input mixer; three-input emitter coupled logic; Bipolar Junction Transistor.

INTRODUCTION

Nonlinear operations on analog signals are performed in various stages of communication, control, and instrumentation systems (Bryant, 2013; Gray *et al.*, 2010; Herath, 2009; Razavi *et al.*, 2001). These operations include multiplication, modulation, demodulation, frequency synthesis, and logic operations. Most commonly used circuit for such operations is the Gilbert Four-Quadrant Multiplier (Nikseresht *et al.*, 2017; Quintero, 2014; Gray *et al.*, 2010; Chien, 2006; Can, 1999; Gilbert *et al.*, 1974; Gilbert *et al.*, 1968). This multiplier circuit can multiply two small input signals. The input signals can operate in all four quadrants (any polarity). The four-quadrant multiplier input can be modified to accommodate large input signals (Gray *et al.*, 2010). Furthermore, Gilbert four-quadrant multiplier circuit topology can be extended to multiply arbitrary number of input signals (Hong *et al.*, 2016; Kimura, 1994; Choma, 1981). Corresponding circuit topology features pairs of differential pairs equal to the number of inputs whose inputs are cross connected and outputs are connected in parallel, “stacked” on top of one another between the load and the bottom most differential pair (Hong, *et al.*, 2016). The multiplier circuit can be realized using bipolar junction transistor (BJT) or metal oxide semiconductor (MOS) technologies (Bryant, 2013; Chien, 2006; Can, 1999; Keating, 1998; Razavi *et al.*, 1994; Blut *et al.*, 1986). This study presents a three input (eight octant) multiplier circuit topology that uses BJT technology. The advantage of the proposed circuit topology over the existing circuit topologies is that in this

topology output signal polarity can be flipped using an external trigger. The drawback is the increase in number of transistors used in the circuit.

Theory

The output currents of the emitter coupled pair shown in the Figure 1 is related to the input voltage V by (Gray *et al.*, 2010; Razavi, 2001)

$$I_{c1} = \frac{I_{EE}}{1 + e^{-\frac{V}{V_T}}}; I_{c2} = \frac{I_{EE}}{1 + e^{\frac{V}{V_T}}} \quad (1)$$

Figure 1: Emitter coupled pair.

where V_T is the thermal voltage and I_{EE} is the tail current. The base current (I_b) $\ll I_c$ where I_c is the collector current. The difference between output (Gray *et al.*, 2010) currents of the emitter coupled pair is given by

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE} \tanh\left(\frac{V}{V_T}\right) \quad (2)$$

In the four quadrant (Gilbert) multiplier circuit shown in the Figure 2 the difference between the output currents is given by (Gray *et al.*, 2010; Chien, 2006; Gilbert, 1974; Gilbert, 1968).

$$\Delta I^G = I_{c3+5} - I_{c4+6} = I_{EE} \tanh \frac{V_1^G}{2V_T} \tanh \frac{V_2^G}{2V_T} \quad (3)$$

Here V_1^G and V_2^G are two inputs respectively. In order to obtain the result given in (3) result (1) is directly applied to the upper transistor layers of the circuit shown in the figure 2. It is possible to do that because when deriving (1) there is no condition that I_{EE} should be derived from a current source.

The proposed eight-octant multiplier circuit is shown in

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Figure 2: Four quadrant (Gilbert) multiplier circuit.

Figure 3: Proposed eight-octant multiplier circuit topology.

the Figure 3. The basic circuit consists of 14 bipolar junction transistors. They are arranged into three layers of emitter coupled pairs. The bottom layer consists of transistors Q_1 and Q_2 . The middle layer consists of transistors Q_3 , Q_4 , Q_5 , and Q_6 . The top layer consists of transistors Q_7 , Q_8 , Q_9 , Q_{10} , Q_{11} , Q_{12} , Q_{13} , and Q_{14} . Transistors in each layer are identical. The collectors of the top layer of transistors are tied into two groups where collectors of Q_7 , Q_9 , Q_{11} , and Q_{13} are tied together and the collector of Q_8 , Q_{10} , Q_{12} , and Q_{14} are tied together. Three input signals are applied between bases of the emitter coupled pairs in each layer as shown in Figure 3. In the following DC analysis it is assumed that the output resistance of the biasing current source and the output resistance of transistors are negligible. The output voltage (V_{out}) is given by,

$$\begin{aligned} V_{out} &= [V_{cc} - \bar{I}R_c] - [V_{cc} - IR_c] \\ V_{out} &= [I - \bar{I}]R_c \\ V_{out} &= \Delta I R_c \end{aligned} \quad (4)$$

Where I and $\bar{I}$ are as shown in the Figure 3. According to the Figure 3.

$$\Delta I = I_{c7} + I_{c9} + I_{c11} + I_{c13} - [I_{c8} + I_{c10} + I_{c12} + I_{c14}] \quad (5)$$

From (1) it can be deduced that,

$$\begin{aligned} I_{c7} &= \frac{I_{c3}}{1 + e^{-\frac{V_1}{V_T}}}; I_{c8} = \frac{I_{c3}}{1 + e^{\frac{V_1}{V_T}}} \\ I_{c9} &= \frac{I_{c4}}{1 + e^{\frac{V_1}{V_T}}}; I_{c10} = \frac{I_{c4}}{1 + e^{-\frac{V_1}{V_T}}} \end{aligned} \quad (6)$$

$$\begin{aligned} I_{c11} &= \frac{I_{c5}}{1 + e^{-\frac{V_1}{V_T}}}; I_{c12} = \frac{I_{c5}}{1 + e^{\frac{V_1}{V_T}}}; \\ I_{c13} &= \frac{I_{c6}}{1 + e^{\frac{V_1}{V_T}}}; I_{c14} = \frac{I_{c6}}{1 + e^{-\frac{V_1}{V_T}}} \end{aligned}$$

With a similar argument it can be deduced that

$$I_{c3} = \frac{I_{c1}}{1 + e^{-\frac{V_2}{V_T}}}; I_{c4} = \frac{I_{c1}}{1 + e^{\frac{V_2}{V_T}}}; I_{c5} = \frac{I_{c2}}{1 + e^{\frac{V_2}{V_T}}}; I_{c6} = \frac{I_{c2}}{1 + e^{-\frac{V_2}{V_T}}} \quad (7)$$

and

$$I_{c1} = \frac{I_{EE}}{1 + e^{-\frac{V_3}{V_T}}}; I_{c2} = \frac{I_{EE}}{1 + e^{\frac{V_3}{V_T}}} \quad (8)$$

Let $\frac{V_1}{V_T} = x_1$, $\frac{V_2}{V_T} = x_2$, and $\frac{V_3}{V_T} = x_3$.

Then from (5), (6), (7), and (8)

$$\Delta I = I_{EE} \left\{ \begin{array}{l} \frac{1}{\frac{1+e^{-x_1}}{1+e^{-x_2}} \frac{1+e^{-x_3}}{1+e^{-x_3}}} + \frac{1}{\frac{1+e^{x_1}}{1+e^{x_2}} \frac{1+e^{x_3}}{1+e^{x_3}}} \\ + \frac{1}{\frac{1+e^{-x_1}}{1+e^{-x_2}} \frac{1+e^{x_3}}{1+e^{x_3}}} + \frac{1}{\frac{1+e^{x_1}}{1+e^{x_2}} \frac{1+e^{-x_3}}{1+e^{-x_3}}} \\ - \frac{1}{\frac{1+e^{x_1}}{1+e^{-x_2}} \frac{1+e^{-x_3}}{1+e^{-x_3}}} - \frac{1}{\frac{1+e^{-x_1}}{1+e^{x_2}} \frac{1+e^{x_3}}{1+e^{x_3}}} \\ - \frac{1}{\frac{1+e^{-x_1}}{1+e^{x_2}} \frac{1+e^{-x_3}}{1+e^{-x_3}}} - \frac{1}{\frac{1+e^{x_1}}{1+e^{-x_2}} \frac{1+e^{x_3}}{1+e^{x_3}}} \end{array} \right\} \quad (9)$$

$$\Delta I = I_{EE} \left\{ \begin{array}{l} \frac{1}{\frac{1+e^{-x_1}}{1+e^{-x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \\ + \frac{1}{\frac{1+e^{x_1}}{1+e^{x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \\ + \frac{1}{\frac{1+e^{-x_1}}{1+e^{x_2}} \left[\frac{1}{1+e^{x_3}} - \frac{1}{1+e^{-x_3}} \right]} \\ + \frac{1}{\frac{1+e^{x_1}}{1+e^{-x_2}} \left[\frac{1}{1+e^{x_3}} - \frac{1}{1+e^{-x_3}} \right]} \end{array} \right\} \quad (10)$$

$$\text{As } \tanh \frac{x}{2} = \frac{1}{1+e^{-x}} - \frac{1}{1+e^x}$$

$$\Delta I = I_{EE} \tanh \frac{x_3}{2} \left\{ \begin{array}{l} \frac{1}{\frac{1+e^{-x_1}}{1+e^{-x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \\ + \frac{1}{\frac{1+e^{x_1}}{1+e^{x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \\ - \frac{1}{\frac{1+e^{-x_1}}{1+e^{x_2}} \left[\frac{1}{1+e^{x_3}} - \frac{1}{1+e^{-x_3}} \right]} \\ - \frac{1}{\frac{1+e^{x_1}}{1+e^{-x_2}} \left[\frac{1}{1+e^{x_3}} - \frac{1}{1+e^{-x_3}} \right]} \end{array} \right\} \quad (11)$$

$$\Delta I = I_{EE} \tanh \frac{x_3}{2} \left\{ \begin{array}{l} \frac{1}{\frac{1+e^{-x_1}}{1+e^{-x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \\ - \frac{1}{\frac{1+e^{x_1}}{1+e^{x_2}} \left[\frac{1}{1+e^{-x_3}} - \frac{1}{1+e^{x_3}} \right]} \end{array} \right\} \quad (12)$$

$$\Delta I = I_{EE} \tanh \frac{x_3}{2} \tanh \frac{x_2}{2} \tanh \frac{x_1}{2} \quad (13)$$

By substituting back the values for x_1 , x_2 , and x_3 we get

$$\Delta I = I_{EE} \tanh \frac{V_3}{2V_T} \tanh \frac{V_2}{2V_T} \tanh \frac{V_1}{2V_T} \quad (14)$$

From (4) and (14)

$$V_{out} = I_{EE} R_c \tanh \frac{V_3}{2V_T} \tanh \frac{V_2}{2V_T} \tanh \frac{V_1}{2V_T} \quad (15)$$

For $V_1, V_2, V_3 \ll V_T$,

$$V_{out} \approx I_{EE} R_c \frac{V_1 V_2 V_3}{8V_T^3} \quad (16)$$

Above analysis proves that for small input signals the output voltage of the circuit shown in the Figure 3 is proportional to the multiplication of three input signals where $I_{EE} R_c / 8V_T^3$ is the proportionality constant. As the analysis does not impose any restriction with regard to the polarity of the input signals this multiplier can operate in all the eight octants of a three dimensional coordinate system.

The circuit shown in the Figure 3 can be modified to multiply large input signals by pre-distorting the input signal as shown in the Figure 4 where K is a constant (Gray *et al.*, 2010).

Figure 4: Pre-distortion of the input signal.

With that modification

$$V_{out} = I_{EE} R_c K^3 V_1 V_2 V_3 \quad (17)$$

In the circuit shown in the Figure 3 if collectors of Q_1 and Q_2 are cross connected respectively to coupled emitters of $Q_3 - Q_4$ and $Q_5 - Q_6$ then the output voltage

$$V_{out} \approx -I_{EE} R_c \frac{V_1 V_2 V_3}{8V_T^3} \quad (18)$$

Therefore by toggling the connections of the collectors of Q_1 and Q_2 between direct and cross connection through an external trigger, as shown in the Figure 5, it is possible to change the polarity of the output signal.

In practical applications the current source can be realized using a current mirror (Gray *et al.*, 2010).

Figure 5: Switching circuit to direct and cross connect collectors of the transistors Q_1 and Q_2 .

RESULTS AND DISCUSSION

As discussed in the introduction, the proposed multiplier circuit can be used as (a) eight-octant analog multiplier (b) switch that will control the output of a two input multiplier (c) three input mixer or (d) Three input emitter coupled logic circuit. Following simulation results discuss each of the above applications.

The circuit shown in the Figure 3 was implemented using quite universal circuit simulator (Qucs) open source circuit simulation software. In all the simulations $I_{EE} = 10 \text{ mA}$, $R_c = 1 \text{ k}\Omega$, V_T is considered to be 26 mV for all simulations except thermal simulation.

Small input signals are used so that linear approximation

is valid. The simulation of thermal performance and noise performance were carried out using LTspice freeware.

Eight-octant analog multiplier

Following signals were applied to the input of the circuit

$$\begin{aligned} V_1 &= 5 \sin(2000\pi t) \text{ mV} \\ V_2 &= 10 \sin(2000\pi t) \text{ mV} \\ V_3 &= 15 \sin(2000\pi t) \text{ mV} \end{aligned} \quad (19)$$

According to (16) the expected output is

$$V_{out} = 53 (\sin 2\pi 1000t)^3 \text{ mV} \quad (20)$$

Figure 6 (a) shows the simulated output signal which is similar to the predicted output shown in the Figure 6 (b.)

In order to verify that multiplication can be done in all eight octants signals similar to the ones used in the previous example but separated from each other by $\frac{2\pi}{3}$

phase shift were applied to inputs. The expected output signal is $-13.25 \sin(2\pi 3000t) \text{ mV}$. Figure 7 (a) shows the output signal in the time domain and figure 7 (b) shows the output signal in the frequency domain. It is evident that multiplication of the input signals has occurred as expected.

In order to observe the behavior of the circuit when the input signals are large, signals $50 \sin(2000\pi t) \text{ mV}$, $100 \sin(2000\pi t + \frac{2\pi}{3}) \text{ mV}$, and

$150 \sin(2000\pi t + \frac{4\pi}{3}) \text{ mV}$ were used as the input signals for the circuit shown in the figure 3 and the corresponding output signal was observed. Figure 8 (a) shows the output signal in the time domain. As expected, nonlinear distortions can be observed in the output signal. Corresponding frequency domain representation is given in the figure 8 (b).

Signals shown in Figure 9 (a) were applied to the three input ports. The magnitudes of the input signals during non-zero voltage levels are 5 mV, 10 mV, and 15 mV. As shown in the Figure 9 (b) output signal is non-zero when all the inputs are non-zero.

Figure 6: Three input multiplier simulated output (a) and expected output (b) with sinusoidal inputs.

Figure 7: Three input multiplier simulated output in (a) time and (b) frequency domain when the input signals are $\frac{2\pi}{3}$ apart in phase.

Figure 8: Three input multiplier simulated output in (a) time and (b) frequency domain when the input signals are large and $\frac{2\pi}{3}$ apart in phase.

Signals shown in the Figure 10 (a) were applied to the three input ports. The magnitudes of the input signals during non-zero voltage levels are 100 mV, 200 mV, and 300 mV. As shown in the Figure 10 (b) output signal is non-zero when all the inputs are non-zero. Because the three input signals are much larger than $V_T (= 26 \text{ mV})$ the circuit operates in the nonlinear region.

The circuit shown in the Figure 3 can be used as a two input multiplier with an enable disable switch. Figure 11 (a) and (b) show the input and output signals in such a scenario. It is necessary to amplify the output signal with a gain equal to the inverse of the amplitude of the pulse.

Three input mixer

Following signals were applied to the input of the circuit

$$\begin{aligned} V_1 &= 10 \sin(2\pi f_1 t) \text{ mV} \\ V_2 &= 10 \sin(2\pi f_2 t) \text{ mV} \\ V_3 &= 10 \sin(2\pi f_3 t) \text{ mV} \end{aligned} \quad (21)$$

If three signals are multiplied by the circuit, the output signal should contain frequencies $f_1 + f_2 + f_3$, $f_1 + f_2 - f_3$, $f_1 + f_3 - f_2$, and $f_1 - f_2 - f_3$. Therefore, if $f_1 = 3 \text{ kHz}$, $f_2 = 6 \text{ kHz}$, and $f_3 = 12 \text{ kHz}$ then the expected output frequency components are 21 kHz, 3 kHz, 9 kHz, and 15 kHz. Figure 12 shows the time domain and frequency domain signal of the output.

Figure 9: Three input multiplier output (b) with inputs as shown in (a).

Figure 10: Three input multiplier output (b) with inputs as shown in (a).

Figure 11: Two input multiplier with enable disable switch outputs (a) with output shown in (b).

Figure 12: Three input mixer output signal time domain (a) and frequency domain (b).

Figure 13: Three input mixer output signal time domain (a) and frequency domain (b).

If $f_1 = 3 \text{ kHz}$, $f_2 = 6 \text{ kHz}$, and $f_3 = 9 \text{ kHz}$ then the expected output frequency components are 18 kHz , 12 kHz , and 6 kHz . Figure 13 shows the time domain and frequency domain signal of the output.

Three input AND logic

The circuit shown in the Figure 3 can be used as a 3-input AND gate with unipolar signaling. In that case the circuit operates in the nonlinear region. The truth table of 3-input AND gate is shown in the Table 1.

Table 1: Truth table of the 3-input AND gate.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Figure 14 shows the input and output waveforms of the circuit during 3-input AND operation. Large input signals can be applied to the circuit in this case because the circuit operates in the nonlinear region. This operation is possible when unipolar signaling is used. It is possible to obtain $A.B.C$ if collectors of Q_1 and Q_2 are cross connected respectively to coupled emitters of $Q_3 - Q_4$ and $Q_5 - Q_6$ in the circuit as shown in the Figure 5.

Three input XOR logic

The circuit shown in the Figure 3 can be used as a 3-input XOR gate with bipolar signaling. Inverse logic is possible with reconnection of circuit. In that case the circuit operate in the nonlinear region. The truth table of 3-input AND gate is shown in the Table 2.

Figure 15 shows the input and output waveforms of the circuit during 3-input XOR operation. Large input signals can be applied to the circuit in this case because the circuit operates in the nonlinear region. This operation is possible for the bipolar signaling.

Figure 14: Inputs and output of the 3-input AND operation of the circuit.

Table 2: Truth table of the 3-input XOR gate.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 15: Inputs and output of the 3-input XOR operation of the circuit.

If in the circuit shown in the Figure 3 collectors of Q_1 and Q_2 are cross connected respectively to coupled emitters of $Q_3 - Q_4$ and $Q_5 - Q_6$ as shown in the Figure 5 it is

possible to achieve $\overline{A \oplus B \oplus C}$ operation.

Thermal performance

The following simulations were carried out to observe the thermal performance of the circuit. The output of the three input multiplier as shown in the Figure 6 was observed by varying the temperature between -25°C to 100°C . Figure 16 shows the observed results. The frequency of all the input signals considered in here are same. It was observed that the amplitude of the signal decline with the increase of temperature. According to (16) output voltage is inversely proportional to V_T^2 and proportional to R_C . Output behavior can be explained by the fact that V_T is proportional to the absolute temperature. Effect of the variation of R_C with temperature, as seen from the simulation results, is small compared to the effect of the variation of V_T .

The performance of the three input mixture for three different frequencies similar to the simulation result shown in the Figure 12 was evaluated for its thermal performance. It was observed, as predicted, that the output voltage reduces with the increase in temperature. The time domain and frequency domain representation for different temperature values are shown Figure 17 and Figure 18.

Noise Performance

The circuit was evaluated for its noise performance where $\pm 10\%$ fluctuations were introduced to the supply voltage (V_{EE}) and tail current (I_{EE}). Figure 19 and Figure 20 show the time domain and frequency domain output after the fluctuations are introduced.

Even though there are fluctuations of the output voltage due to supply noise and ground noise the output signal closely resembles the signal shown in the Figure 6.

Figure 16: Thermal performance of the three input mixture. **Figure 17:** Thermal performance of the three input mixture for three different frequencies.

Figure 18: Frequency domain representation of the thermal performance of the three input mixture for three different frequencies.

Figure 19: Time domain representation of the Three input mixture output under supply and ground noise.

Figure 20: Frequency domain representation of the Three input mixture output under noise.

Figure 21: Three input mixture output for input SNR = -92 dB.

Figure 22: Three input mixture output for input SNR = -3.7 dB.

Figure 23: Three input mixture output for input SNR = -0.53 dB.

The circuit was evaluated for its performance by varying the Signal to Noise Ratio (SNR) value at the input and it was observed that the performance of the circuit improves with the increasing SNR at the input. The Figures 21, 22, 23 show the output of three input multiplier for different SNR values.

CONCLUSIONS

This study presents a circuit topology for an eight octant analog multiplier. It is possible to invert the output signal of the circuit by cross connecting two BJT transistors that are directly connected to the current source. Simulations have shown that the circuit can be used as (a) eight-octant analog multiplier (b) switch that will control the output of a two input multiplier (c) three input mixer or (d) Three input emitter coupled logic circuit. In the simulations input signals are small in the cases (a), (b), and (c). By applying the modification proposed in the theory section it should be possible to operate the circuit for large input signals too. Thermal and noise simulations showed that the circuit operates as predicted for moderate variations of temperature and for low noise levels.

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REFERENCES

- Blut, K., Wallinga, H. (1989). A CMOS Four-Quadrant Analog Multiplier. *IEEE Journal of Solid-State Circuits* **21**(3): 430-435.
- Bryant, J. (2013). Multipliers vs. Modulators. *Analog Dialogue* **47**(2): 3-4.
- Can, S. (1999). Folded Analog Signal Multiplier. *US Patent*, No. 5,877, 974.
- Chien, G. (2006). Gilber Cell and Method Thereof. *US Patent*, No. 7,088, 982.
- Choma, J. (1981). A Three-Level Broad-Banded Monolithic Analog Multiplier. *IEEE Journal of Solid-State Circuits* **16**(4): 392-399.
- Gilbert, B. (1968). A Precise Four-Quadrant Multiplier with Sub nano-second Response. *IEEE Journal of Solid-State Circuits* **3**: 365 - 373.
- Gilbert, B. (1974). A New High-Performance Monolithic Multiplier Using Active Feedback. *IEEE Journal of Solid-State Circuits* **9**: 364 - 373.
- Gray, P. R., Hurst, P. J., Lewis, S. H., and Meyer, R. G. (2010). Analysis and Design of Analog Integrated Circuits. John Wiley, 704 – 712pp.
- Herath, V.R. (2011). *ASIC Design for a Coherent Optical Receiver DSPU*. LAP Lambert.
- Hong, B., and Hajimiri, A. (2016). Analysis of a Balanced Analog Multiplier for an Arbitrary Number of Signed Inputs. *International Journal of Circuit Theory and Applications*. **45** (4): 1-19.
- Keating, P. V. (1998). Emitter Coupled Logic Gate. *US Patent*, No. 5,831, 454.
- Kimura, K. (1994). Some circuit design techniques using two cross coupled, emitter coupled pairs. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* **41**(5): 411423.
- Nikseresht, S., Azhari, S.J., and Danesh, M. (2017). High bandwidth four-quadrant analog multiplier. *Iranian Conference on Electrical Engineering*, 210-215pp.
- Quinetto, R.F.F. (2014). Design of Four-Quadrant Analog Multipliers Robust PVT Variations. *National Institute for Astrophysics, Optics and Electronics, Mexico*.
- Razavi, B., Ota, Y., and Swartz, R. G. (1994). Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits. *IEEE Journal of Solid-State Circuits* **29**(3): 332-339.
- Razavi, B. (2001). Design of Analog CMOS Integrated Circuits, McGraw Hill, 448– 452pp.